ABSTRACT OF THE DISCLOSURE

An image processing apparatus which eliminates noise which occurs due to the influence of output from a parallel bus drive circuit added to an output final stage circuit of signal processor or the like. A delay circuit 110 which delays a video signal is inserted into a VTR signal processor such that a data transition point of particular bit in a bit array indicating horizontal-directional start and end positions of video signal data, added during a horizontal retrace period of a digital recording format video signal, does not overlap with a period for sampling a feedthrough period and a photoelectric conversion signal period in a correlated double sampling circuit.